WHAT IS CLAIMED IS:

1. A microprocessor comprising:

a dispatch unit configured to forward instructions comprising an instruction group to at least one functional unit for execution;

sampling logic configured to select an instruction from the instruction group for performance monitoring based upon the slot of the instruction group in which the selected instruction is located; and

a performance monitor unit configured to receive from the functional unit at least one signal indicative of an event occurring during execution of an instruction and further configured to record the occurrence of the event if the instruction was selected for performance monitoring.

2. The microprocessor of claim 1, wherein the sampling logic generates a selection vector comprising a single asserted bit indicative of the instruction group slot in which the selected instruction is located.

3. The microprocessor of claim 2, wherein an initial condition of the selection vector is derived from a programmable input mask.

4. The microprocessor of claim 3, wherein the input mask is transferable to a selection mask from which the selected instruction is determined and wherein the contents of the selection mask vary with time.

5. The microprocessor of claim 4, wherein selection mask is applied to a filter to produce the selection vector, wherein the filter selects a single asserted bit from the asserted bits in the selection mask.

6. The microprocessor of claim 5, wherein the filter selects the most significant asserted bit in the selection mask.

7. The microprocessor of claim 1, wherein the sampling logic includes a shift register comprising a bit position corresponding to each instruction group slot and wherein the selected instruction is determined from the shift register.

8. The microprocessor of claim 7, wherein the shift register shifts periodically and further wherein shifts in the shift register affect the selected vector.

9. The microprocessor of claim 1, wherein the sampling logic sets a bit indicative of the selected instruction in a completion table entry corresponding to the instruction group.

10. A data processing system including processor, memory, display, and input means, the processor comprising:

a dispatch unit configured to forward instructions comprising an instruction group to at least one functional unit for execution;

sampling logic configured to select an instruction from the instruction group for performance monitoring based upon the slot of the instruction group in which the selected instruction is located; and

a performance monitor unit configured to receive from the functional unit at least one signal indicative of an event occurring during execution of an instruction and further

configured to record the occurrence of the event if the instruction was selected for performance monitoring.

11. The data processing system of claim 10, wherein the sampling logic generates a selection vector comprising a single asserted bit indicative of the instruction group slot in which the selected instruction is located.

12. The data processing system of claim 11, wherein an initial condition of the selection vector is derived from a programmable input mask.

13. The data processing system of claim 12, wherein the input mask is transferable to a selection mask from which the selected instruction is determined and wherein the contents of the selection mask vary with time.

14. The data processing system of claim 13, wherein the selection mask is applied to a filter to produce the selection vector, wherein the filter selects a single asserted bit from the asserted bits in the selection mask.

15. The data processing system of claim 1, wherein the sampling logic includes a shift register comprising a bit position corresponding to each instruction group slot and wherein the selected instruction is determined from the shift register.

16. A method of executing instructions in a microprocessor, comprising:

grouping a set of instructions into an instruction group and assigning an entry corresponding to the instruction group in a completion table;

selecting an instruction from the instruction group for performance monitoring based upon the instruction position within the instruction group; and

recording the occurrence of an event associated with the selected instruction when the selected instruction is executed.

17. The method of claim 16, wherein the selected instruction position varies from instruction group to instruction group.

18. The method of claim 16, selecting the instruction for performance monitoring includes generating a selection vector with a single asserted bit indicative of the selected instruction.

19. The method of claim 18, wherein generating the selection vector includes filtering all but one asserted bit from a selection mask comprising at least one asserted bit.

20. The method of claim 19, wherein filtering all but one asserted bit from the selection mask includes clearing all asserted bits except for the most significant asserted bit in the selection mask.